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For

METHOD AND SYSTEM FOR USING ONE OR MORE ADDRESS BITS AND AN INSTRUCTION TO INCREASE AN INSTRUCTION SET

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CONFIDENTIAL

METHOD AND SYSTEM FOR USING ONE OR MORE ADDRESS BITS AND AN INSTRUCTION TO INCREASE AN INSTRUCTION SET

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention generally relates to computer architecture. More particularly, the present invention relates to the field of increasing an instruction set by using one or more address bits and an instruction.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the present invention.

Figure 1 illustrates an instruction, a corresponding address, and a plurality of concatenations of a portion of the corresponding address and the instruction in accordance with an embodiment of the present invention.

Figure 2 illustrates a system in accordance with an embodiment of the present invention.

Figure 3 illustrates a flow chart showing a method of processing an instruction in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to embodiments of the present invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with these embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one of ordinary skill in the art that the present invention may be practiced without these specific details.

At any point in time, a processor executes a particular function chosen from a set of functions. The particular function chosen is determined by how the processor decodes each instruction in memory. Thus, the "meaning" of an instruction is the selection of particular function as a result of the instruction decoding. Traditionally, the meaning of an instruction depends solely on the bits forming the instruction word stored in memory. In accordance with one embodiment of the present invention, the meaning of an instruction is additionally dependent on some or all of the address at which the instruction is stored.

Figure 1 illustrates an instruction 10, a corresponding address 20 at which instruction 10 is stored, and a plurality of concatenations 30 and 40 of a portion of the

corresponding address 20 and the instruction 10 in accordance with an embodiment of the present invention. Rather than increasing an instruction set by increasing the size of the instruction 10, the instruction set is increased by utilizing one or more bits from the corresponding address 20 of the instruction 10 in memory.

The instruction 10 has m bits. Exemplary values for m are 16, 32, 64, and 128. The instruction 10 includes an opcode portion 5 and a portion 7 for register identifiers, an immediate, etc.

The corresponding address 20 is provided to memory to access the instruction 10. The corresponding address 20 has k bits. Exemplary values for k are 16, 32, 64, and 128.

In accordance with the present invention, a plurality of possible meanings is associated with instruction 10. That is, the same bit pattern of the instruction 10 can lead to any one of several meanings which then controls instruction execution by a processor. The desired meaning is determined by concatenating one or more bits from the corresponding address 20 to the instruction 10. As shown in Figure 1, the concatenation 30 is comprised of b_2 from the corresponding address 20 concatenated to the instruction 10. Hence, if b_2= 0, the instruction 10 obtains the meaning1. Similarly, if b_2= 1, the instruction 10 obtains the meaning2. For example, meaning1 can correspond to an integer instruction while meaning2 can corresponding to a floating point instruction. Moreover, a particular bit from the corresponding address 20

can be selected whose value would indicate whether the corresponding address 20 was an even address or an odd address.

In one embodiment, the concatenation 40 is comprised of b_2b_1 from the corresponding address 20 concatenated to the instruction 10. Hence, if b_2b_1= 00, the instruction 10 obtains the meaning1. If b_2b_1= 01, the instruction 10 obtains the meaning2. Moreover, if b_2b_1= 10, the instruction 10 obtains the meaning3. Similarly, if b_2b_1= 11, the instruction 10 obtains the meaning4. It should be understood that other bits from the corresponding address 20 can be concatenated to the instruction 10.

The one or more bits from the corresponding address 20 can affect the meaning of the opcode portion 5 and the portion 7 for register identifiers, an immediate, etc. Moreover, the instruction set is increased without increasing the size of the instruction 10 in memory, or storing additional instructions.

Figure 2 illustrates a system 200 in accordance with an embodiment of the present invention. The system 200 includes a memory unit 230, a processor 210, and a compiler 240.

The memory unit 230 stores a plurality of instructions at a plurality of addresses. A plurality of possible meanings can be associated with each instruction. The compiler 240 generates the plurality of instructions and stores each instruction at an appropriate address in the memory unit 230 to facilitate the concatenation operation

that determines the meaning of the instruction. For example, if an instruction needs to be stored at an even address to obtain a desired meaning, the compiler or translator ensures that it is stored at an even address. The compiler or translator does similar work for other alignments.

The processor 210 includes a front-end portion 212 and a backend pipeline portion 214. The front-end portion 212 includes a program counter 216 and a concatenation unit for concatenating a portion of the address to the instruction. Moreover, the front-end portion 212 provides the address to the memory unit 230 and receives the instruction from the memory unit 230. The backend pipeline portion 214 executes the concatenation comprised of a portion of the address and the instruction.

As described above, any portion of the address can be concatenated to the instruction to determine its meaning. Here, one bit from the address (32 bits) is concatenated to the instruction1 (32 bits) to form a concatenation (or extended instruction) having 33 bits. The concatenation (33 bits) is sent to the backend pipeline portion 214. The value of the bit from the address determines the meaning of the instruction.

Figure 3 illustrates a flow chart showing a method 300 of processing an instruction in accordance with an embodiment of the present invention. Reference is made to Figure 2.

At Step 310, the processor 210 fetches the instruction using a corresponding address from the memory unit 230. A plurality of possible meanings is associated with the instruction.

Continuing, at Step 320, the processor 210 receives the instruction. Moreover, the processor concatenates a portion of the corresponding address to the instruction to form a concatenation (or extended instruction). One or more bits of the corresponding address can be concatenated to the instruction.

At Step 330, the processor 210 executes the concatenation (or extended instruction). The portion of the corresponding address contributes to determining the meaning for the extended instruction from the possible meanings.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.